Amendments to the Specification:

Please replace paragraph beginning on page 9, line 8 with the following amended paragraph:

In one implementation, the reconfigurable logic core 153 is programmed as a hardcoded vector processor in front of the general purpose processor cores 151, to do the bulk of the processing and to `parallelize` the data output This parallel data output would then be fed simultaneously to all general-purpose processor cores 151 (rather than in series) for additional DSP operation. The reconfigurable logic core 153 pre-packages the data so that the processor cores 151 working in parallel can efficiently process the RF data stream. The general-purpose processor cores 151, upon detecting that a high-speed standard is being used, select this parallel mode. The processor cores 151 also selects the ASIC preprocessor function of the reconfigurable logic core 153, which though hardcoded can still be customized on the fly by selecting one or more architecture selection switches. In one embodiment, a router 190 is used to de-correlate the incoming data such as data from 802.11 or GPRS transmitters and send the de-correlated data to the processor cores 151. Typically, data coming is `related`, so a block of, for example, 200 bits is needed to reconstruct the original signal. The router 190 takes this data-word and converts the stream into parallel streams that are not time-correlated so that the processors can operate in parallel.

Please replace paragraph beginning on page 12, line 7 with the following amended paragraph:

The reconfigurable processor core 150 controls the cellular radio core 110 and the short-range wireless transceiver core 130 to provide a seamless dual-mode network integrated circuit that operates with a plurality of distinct and unrelated communications standards and protocols such as Global System for Mobile Communications (GSM), General Packet Radio Service (GPRS), Enhance Data Rates for GSM Evolution (Edge) and Bluetooth™. The cell ~~phone~~ radio core 110 provides wide area network (WAN) access, while the short-range wireless transceiver core 130 supports local area network (LAN) access. The reconfigurable processor core 150 has embedded read-only-memory (ROM) containing software such as IEEE802 11, GSM, GPRS, Edge, and/or Bluetooth™ protocol software, among others.

Please replace paragraph beginning on page 12, line 17 with the following amended paragraph:

In one embodiment, the cellular radio core 110 includes a transmitter/receiver section that is connected to an off-chip antenna ~~(not shown)~~. The transmitter/receiver section is a direct

conversion radio that includes an I/Q demodulator, transmit/receive oscillator/clock generator, multi-band power amplifier (PA) and PA control circuit, and voltage-controlled oscillators and synthesizers. In another embodiment of the transmitter/receiver section ~~112~~, intermediate frequency (IF) stages are used. In this embodiment, during cellular reception, the transmitter/receiver section converts received signals into a first intermediate frequency (IF) by mixing the received signals with a synthesized local oscillator frequency and then translates the first IF signal to a second IF signal. The second IF signal is hard-limited and processed to extract an RSSI signal proportional to the logarithm of the amplitude of the second IF signal. The hard-limited IF signal is processed to extract numerical values related to the instantaneous signal phase, which are then combined with the RSSI signal.

Please replace paragraph beginning on page 13, line 17 with the following amended paragraph:

Turning now to the short-range wireless transceiver core 130, the short-range wireless transceiver core 130 contains a radio frequency (RF) modem core 132 that communicates with a link controller core 134. The processor core 150 controls the link controller core 134 In one embodiment, the RF modem core 132 has a direct-conversion radio architecture with integrated VCO and frequency synthesizer The RF-unit 132 includes an RF receiver connected to an analog-digital converter (ADC), which in turn is connected to a modem ~~116~~ performing digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicing operations. For transmission, the modem is connected to a digital to analog converter (DAC) that in turn drives an RF transmitter.

Please replace paragraph beginning on page 17, line 8 with the following amended paragraph:

The system of FIG. [[2]] 1B supports 4 dimensional computing capability. In Dimension 1, each processor is doing a specific separate task. For example, one processor processes Bluetooth signal while another processor handles GPS processing In Dimension 2, each processor is doing tasks in series with the other processors. For example, one processor performs GPRS equalization, moves the data to the next processor which does convolutional decoding, moving the data to the next processor which does vocoder decoding. This way slow, complicated functions like GPRS can be performed.